	Application No.	Applicant(s)
Nation of Alleger Lills	10/023,011	SIX, LAURENT A.
Notice of Allowability	Examiner	Art Unit
	John J. Tabone, Jr.	2133
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. X This communication is responsive to Amendment filedof 01/31/2005.		
2. X The allowed claim(s) is/are <u>21</u> .		
3. The drawings filed on 31 December 2001 are accepted by the Examiner.		
4.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Summary Paper No./Mail Da 08), 7. ☐ Examiner's Amendr	tè
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DETAILED ACTION

1. Newly added claim 21 has been examined. Claims 1-20 have been canceled.

Response to Arguments

2. Applicant's arguments, see Applicant Remarks, filed 01/31/2005, with respect to claims 1-20 and newly added claim 21 have been fully considered and are persuasive.

The Examiner favors the allowance of claim 21.

Allowable Subject Matter

3. Claim 21 is allowed.

The following is an Examiner's Statement of Reason for Allowance.

The present invention relates to a method for providing context save and restore using a test scan chain in an integrated circuit device also having a memory and a state machine.

The claimed invention as set forth in claim 21 recites features such as: providing a scan chain of digital logic components comprised of a plurality of sub-chains; in a test mode, providing an input test data set to the scan chain, and scanning the input test data set through the scan chain, and providing an output test data set as an output of the scan chain; in a first switch mode, linking the sub-chains in parallel with each other and to a device memory, and reading a first functional data set from the memory; in a functional mode, linking the digital logic components with other logic circuitry in

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accordance with an application to be executed by the state machine, and executing the application to generate second functional data; and in a second switch mode, linking the sub-chains in parallel with each other and to the memory; storing the second functional data set in the memory.

The prior art of record teaches providing a scan chain (Fig. 6, 610) of digital logic components comprised of a plurality of sub-chains (Fig. 7, 704); providing an input test data set to the scan chain (Fig. 6, 606), and scanning the input test data set through the scan chain, and providing an output test data set as an output of the scan chain (Fig. 6, 608); linking the sub-chains in parallel with each other (Fig. 7, 704, ¶ 43); linking the digital logic components with other logic circuitry in accordance with an application to be executed by the state machine, and executing the application to generate second functional data (Page 4, ¶ 41-42); Kurtulik et al. (U52002/0125907) is an example of such prior art. The prior arts of record, however, fail to teach, singly or in combination, in a first switch mode, linking the sub-chains in parallel with each other and to a device memory, and reading a first functional data set from the memory as recited in claim 21. The prior arts of record also fail to teach, singly or in combination, in a second switch mode, linking the sub-chains in parallel with each other and to the memory; storing the second functional data set in the memory as recited in claim 21. As such, modification of the prior art of record to include the claimed first switch mode and second switch mode, as described above, can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention

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would have made the necessary modifications to the prior art of record to encompass the **first switch mode** and **second switch mode** set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the **first switch mode** and **second switch mode** as described above.

The Examiner agrees with the Applicant's arguments with regard to these features in view of the arts of record; therefore, the Examiner favors the allowance of claim 21. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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John J. Tabone, Jr.

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